This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A reconfigurable emulation integrated circuit, comprising:

a storage unit comprising a signal inclusion schedule; and

circuitry, coupled to the storage unit, operative to generate and transmit a message outside the emulation integrated circuit, the message comprising a plurality of signals ~~and~~ assembled in accordance with the signal inclusion schedule, wherein the signal inclusion schedule selects the plurality of signals from at least one pin when the message is assembled and specifies the order and frequency of occurrence of each of the plurality of signals in the message.

Claim 2 (previously presented): The reconfigurable emulation integrated circuit of claim 1, wherein signals in a message that are determined to be more critical than other signals occur with greater frequency than signals determined to be less critical in the signal inclusion schedule.

Claim 3 (previously presented): The reconfigurable emulation integrated circuit of claim 1, wherein the message is generated and transmitted in a plurality of clock cycles of an operating clock that is independent of an emulation clock of the plurality of signals.

Claim 4 (previously presented): The reconfigurable emulation integrated circuit of claim 1, wherein the circuitry further includes a parity value generator and wherein the message further comprises a parity value generated by the parity value generator.

Claims 5-8 (canceled)

Claim 9 (currently amended): A reconfigurable integrated circuit, comprising:

a storage unit comprising a signal inclusion schedule for a plurality of signals to be received in a message, the plurality of signals selected from at least one pin when the message is assembled; and

circuitry, coupled to the storage unit, operative to receive and extract the plurality of signals from the message in accordance with the signal inclusion schedule, wherein the signal

inclusion schedule specifies the order and frequency of occurrence of each of the plurality of signals in the message.

Claim 10 (previously presented): The reconfigurable emulation integrated circuit of claim 9, wherein signals in a message that are determined to be more critical than other signals occur with greater frequency than signals determined to be less critical in the signal inclusion schedule.

Claim 11 (previously presented): The reconfigurable emulation integrated circuit of claim 9, wherein the message comprises state values of the plurality of signals.

Claim 12 (previously presented): The reconfigurable emulation integrated circuit of claim 9, wherein the message is received and disassembled in a plurality of clock cycles of an operating clock that is independent of an emulation clock of the plurality of signals.

Claim 13 (previously presented): The reconfigurable emulation integrated circuit of claim 9, wherein a parity value is extracted from the message.

Claim 14 (previously presented): The reconfigurable emulation integrated circuit of claim 13, wherein the circuitry is further configured to generate a parity verification value from the extracted plurality of signals and compare the parity verification value with the extracted parity value.

Claims 15-19 (canceled)

Claim 20 (currently amended): An emulation integrated circuit, comprising:

at least one reconfigurable logic resource;

at least one output pin; and

a message formation and send block in communication with the output pin and the reconfigurable logic resource, the message formation and send block operative to receive multiple output signals from the reconfigurable logic resource and generate a message on the output pin in accordance with a first signal inclusion schedule that selects at least one of the

multiple output signals when the message is generated, wherein the first signal inclusion schedule specifies the order and frequency of occurrence of each of the output signals.

Claim 21 (original): The emulation integrated circuit of claim 20, further comprising:

an input pin; and

a message receive and disassembly block in communication with the input pin and the reconfigurable logic resource, operative to receive a message and extract multiple input signals from the message in accordance with a second signal inclusion schedule.

Claim 22 (original): The emulation integrated circuit of claim 20, further comprising a plurality of output pins and a plurality of message formation and send blocks in communication with the plurality of output pins and the reconfigurable logic resource, each message formation and send block operative to receive multiple output signals from the reconfigurable logic resource and generate a message on the output pin in accordance with a different respective signal inclusion schedule.

Claim 23 (original): The emulation integrated circuit of claim 20, further comprising a plurality of reconfigurable logic resources in communication with the message formation and send block.

Claim 24 (currently amended): An emulation integrated circuit, comprising:

at least one reconfigurable logic resource;

at least one input pin; and

a message receive and disassembly block in communication with the reconfigurable logic resource and the input pin, the message receive and disassembly block operative to receive a message assembled from a selection of multiple input signals from at least one pin when the message is assembled in accordance with a first signal inclusion schedule, wherein the message is received at~~by~~ the at least one input pin and ~~extract~~ the multiple input signals are extracted for the at least one reconfigurable logic resource in accordance with a second signal inclusion schedule, wherein the second signal inclusion schedule specifies the order and frequency of occurrence of each of the input signals.

Claims 25-27 (canceled)

Claim 28 (new) The emulation integrated circuit of claim 24, wherein the first signal inclusion schedule and the second signal inclusion schedule are different signal inclusion schedules.